Hardent and Xilinx Collaborate to Deliver Complete 8K Ready DisplayPort 1.4 IP Subsystem

New IP solution combining Hardent and Xilinx IP will enable pro A/V designers to take advantage of the full DisplayPort 1.4 feature set to support resolutions up to 8K.

MONTREAL (PRWEB) January 31, 2019 -- Hardent, a leading provider of video compression IP cores and Certified member of the Xilinx Alliance Program, today announced the launch of a new DisplayPort™ 1.4 IP subsystem solution developed in collaboration with Xilinx. The VESA-compliant IP subsystem combines Xilinx DisplayPort 1.4 IP and Hardent VESA Display Stream Compression (DSC) and Forward Error Corrector (FEC) IP to meet the requirements of a broad range of DisplayPort pro A/V applications transporting video up to 8K.

DisplayPort 1.4 includes support for VESA DSC 1.2a, a visually lossless video compression technology that increases the DisplayPort data transfer capacity by 3X, while using the same physical link speed. When DSC is used, DisplayPort specifies Forward Error Correction (FEC) to ensure reliable, error-free video transport. With DSC’s bandwidth reduction, the DisplayPort 1.4 standard can be used to transport Ultra High Definition (UHD) and High Dynamic Range (HDR) video streams across a single DisplayPort interface for pro A/V applications such as digital signage, KVM extenders and switchers, high-end projectors, professional video switchers and routers, and test equipment.

Hardent’s DisplayPort 1.4 IP subsystem targets customers using Xilinx® UltraScale™ and UltraScale+™ devices and delivers an out-of-the-box IP solution to help designers achieve a faster time-to-market. “More and more pro A/V applications need to support higher resolutions and greater color depths,” explains Ramesh Iyer, Director, Pro A/V and Broadcast at Xilinx. “We are pleased to have collaborated with Hardent to expand upon our existing DisplayPort IP solution to support the key DisplayPort features needed for 8K.”

The complete DisplayPort 1.4 IP subsystem includes:

- Xilinx Video PHY Controller & DisplayPort 1.4 TX or RX Subsystem IP
- Hardent VESA DisplayPort 1.4 Forward Error Corrector (FEC) TX or RX IP for Xilinx FPGAs
- Hardent VESA Display Stream Compression (DSC) 1.2a Encoder or Decoder IP for Xilinx FPGAs
- Reference design with Vivado Design Suite & SDK project files
- Documentation for each IP
- Comprehensive integration guide
- Software drivers and user application example
- Technical support from the Hardent engineering team

The DisplayPort 1.4 IP subsystem will be demonstrated at Integrated Systems Europe (ISE) in Amsterdam from February 5-8, 2019. The 8K demo will take place at the Xilinx booth in Hall 15, booth number D240. Further information about the DisplayPort 1.4 IP subsystem solution is available on Hardent’s website.

About Hardent
Hardent is a professional services firm providing IP products, engineering services, and training solutions to leading electronics equipment and component manufacturers throughout the world. Hardent works across a
wide variety of industries to develop high-complexity electronic products, improve engineering processes, accelerate products' time-to-market, and provide expert training solutions.
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