IPFlex's DAPDNA-2 Dynamically Reconfigurable Processor Chosen as Key Component in FAST Corporation's High-Speed Image Processing Board

*Using the DAPDNA-2 processor, this board enables switching between multiple image processing methods while system is running, providing high performance and reduced cost.*

(PRWEB) November 30, 2004 -- IPFlex Inc. (headquartered in Tokyo Japan, hereafter referred to as IPFlex) today announced FAST Corporation (headquartered in Kanagawa Japan, hrereafter referred to as FAST) has chosen IPFlex's DAPDNA-2 (see Note 1) Dynamically Reconfigurable Processor (see Note 2) as a key component of the FVDDP01 high-speed image processing board.

In the high-speed data processing needed for machine vision inspection systems, various algorithms are typically assigned to multiple PCs or processing boards, with image data being distributed to network of PCs or boards. Using the DAPDNA-2 processor, FAST supplies its customers a single board that is capable of handling multiple image processing tasks in parallel, as well as changing its inspection methods while system is in operation. Consequently, the board allows customers to reduce the number of PCs and boards needed, thus reducing the cost associated with setting up machine vision inspection systems.

Why the DAPDNA-2?
Today's industrial cameras, which have resolutions above one mega pixel produce large volumes of image data. Same is true for high-precision line sensor cameras and other such imaging devices. However, it is becoming increasingly challenging to achieve the processing speed necessary to handle images larger than VGA size using conventional inspection solutions.

Attempts to solve these problems using solutions other than dynamically reconfigurable processors have included ASIC- and FPGA-based processors. Both these approaches have problems associated with design productivity. ASICs can provide the necessary processing speed, but their circuitry is hard-coded, thus enable to keep up with evolving algorithms. The maximum operating frequency of an FPGA falls off as the size of the circuitry passes a certain point, making it difficult to predict the performance that will be achieved. FPGAs also take a long time to efficiently implement processing algorithms, with the un-deterministic nature of P&R.

To deal with these issues, FAST looked carefully at dynamically reconfigurable processors, which provide easy, flexible modifications to their circuit configurations. The company chose the IPFlex DAPDNA-2, a leading example of such processors, for the development of a high-speed image processing board. The product allows FAST's customers achieve high-speed processing of large volumes of image data, while cutting costs by reducing the numbers of PCs and boards required to perform the necessary tasks.

About the FVDDP01 Board
The FVDDP01 board under development by FAST is the image processing board with a PCI bus, capable of rapidly processing large volumes of image data. The board supports a variety of high-speed image filtering capabilities, such as spatial filter processing, Fourier transforms, and wavelet conversion. This board will realize its full potential in applications such as flat panel display inspection, where a high degree of inspection precision is a must, as well as in the inspections of semiconductor and electronic components.

[About the DAPDNA-2 Dynamically Reconfigurable Processor]
On March 17, 2004, IPFlex introduced the DAPDNA-2, the world's first dynamically reconfigurable
This processor is capable of changing its internal configuration instantly, allowing multiple applications, conventionally implemented using multiple chips, to be implemented using a single chip. The DAPDNA-2 is a dual-core processor, comprised of a high-performance RISC processor core, called the DAP, and the DNA, a two-dimensional array of 376 processing elements (PEs). The DAPDNA-2 can be configured to provide the optimal circuitry for a particular application. This configuration takes place not only when the system is initialized, but can also occur dynamically (in a single clock cycle (see Note 3) while the system is running, to meet the instantaneous needs of the applications implemented by the system.

This unique processor supports high-speed handling of multiple applications in two different ways. With multifunction processing, multiple applications can be called up and executed rapidly. With time-sliced processing, an application can be partitioned into multiple tasks, with one task loading and executing only nanoseconds after the previous task completes.

**Terminology**

Note 1 - DAPDNA - Digital Application Processor / Distributed Network Architecture

Note 2 - Dynamically Reconfigurable Processor: A processor that is able to dynamically switch the circuit configuration within a chip

Note 3 - One clock switching operation is possible by creating configuration information beforehand in the background.

**About FAST Corporation**

FAST Corporation is an image processing equipment maker established in 1982. FAST designs, manufactures, and markets image processing equipment; primarily for the factory automation market (annual sales are 4,000-5,000 units). Recently, FAST has focused attention on inspection systems for flat panel displays, such as LCD and PDP, as well as automation systems that use image processing technology in non-destructive inspection of concrete structures. FAST is also moving into new markets. Through the end of this year, FAST will add to its lineup new products such as high-precision color cameras (area and line) and printed surface inspection equipment. The trend in image processing equipment demand is for smaller equipment, faster speed, more features, and higher precision (higher pixel count). With the choice of the IPFlex DAPDNA-2 for its high-speed image processing board, FAST aims to make a dramatic leap forward in meeting these needs.

**About IPFlex**

IPFlex develops dynamically reconfigurable processors and its integrated development software. Dynamically reconfigurable processor based on Digital Application Processor/Distribute Network Architecture (DAPDNA) is designed as a dual-core processor comprised of a high-performance RISC core and a dynamic reconfigurable processor core, and it is a platform that provides hardware performance while maintaining software flexibility. The DAPDNA dynamic reconfigurable processor series is provided with the DAPDNA-FW II as the integrated software development environment. It provides compilers for algorithms written in MATLAB/Simulink and C with data flow extension, thus realizing high-abstraction level algorithm design and leveraging existing intellectual properties of users. Using DAPDNA can dramatically increase programming productivity and cut cost considerably. For more information, please visit: [http://www.ipflex.com/](http://www.ipflex.com/).

For more information

Miwa Sasaki
Marketing Division

TEL: 03- 5436-3633
Information contained in press releases is up-to-date as of the date of release. Please note that, as such, it is subject to change without prior notice.

IPFlex®, DAPDNA®, and Software-to-Silicon® are registered trademarks of IPFlex in Japan. Other corporate and product names are the trademarks or registered trademarks of their respective owners.

###
Contact Information
Miwa Sasaki
IPFLEX INC.
http://www.ipflex.com
03-5436-3633

Online Web 2.0 Version
You can read the online version of this press release here.